In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A multiprocessor system comprising:

a plurality of data processors, each data processor including:

a data processing core capable of data processing according to program control and memory access,

a memory forming a local portion of a unified memory shared among said plurality of data processors, and

a global memory arbitration logic connected to said data processing core and said memory of each of said data processors, said global memory arbitration logic having a close connection to said data processing core of said corresponding data processor and to said data processing core of at least one other data processor but less than all other data processors and a far connection to said data processing core of additional data processors, said global memory arbitration logic arbitrating access to said ~~close~~ memory forming said local portion of said unified memory granting a first type access to ~~close~~ said data processing cores having said close connection and a second type access different from ~~aid~~ said first type access to ~~far~~ said data processing cores having said far connection.

2. (Currently Amended) The multiprocessor system of claim 1, wherein:

said local portion of said unified memory of each data processor is a dual port memory having a first port and a second port; and

said global memory arbitration logic arbitrating access to said first port of said dual port memory among said ~~close~~ data

processing cores having said close connection thereby providing said first type access and arbitrating access to said second port of said dual port memory among said ~~far~~ data processing cores having said far connection thereby providing said second type access.

Claims 3 and 4. (Canceled)

5. (Currently Amended) The multiprocessor system of claim 2, wherein:

each of said data processors further includes a local memory connected to said data processing core and directly accessible by said data processing core and ~~not~~ neither directly connected to nor directly accessible by said data processing cores of other data processors.

6. (Currently Amended) A multiprocessor system comprising:

a plurality of data processors, each data processor including:

a data processing core capable of data processing according to program control and memory access,

a memory forming a local portion of a unified memory shared among said plurality of data processors having a first port and a second port, and

a global memory arbitration logic connected to said data processing core and said memory of each of said data processors, said global memory arbitration logic having a close connection to said data processing core of said corresponding data processor and to said data processing core of at least one other data processor but less than all other data processors and a far connection to said data processing core of additional data processors, said global memory arbitration logic arbitrating access to said first port of

said dual port memory among said ~~close~~ data processing cores having said close connection thereby providing a first type access and arbitrating access to ~~a~~ said second port of said dual port memory of another data processor among said data processing cores having ~~a~~ said far connection to said global memory arbitration logic of said another data processor thereby providing a second type access.

Claims 7 and 8. (Canceled)

9. (Currently Amended) The multiprocessor system of claim 6, wherein:

each of said data processors further includes a local memory connected to said data processing core and directly accessible by said data processing core and ~~not~~ neither directly connected to nor directly accessible by said data processing cores of other data processors.

10. (Currently Amended) The multiprocessor system of claim 6, wherein:

said plurality of data processors consists of four data processors;

said global memory arbitration logic of each data processor has a close connection to its corresponding data processor and ~~another~~ one other data processor and has a far connection to two other data processors.